Hi3535 H.264 CODEC Processor

# Brief Data Sheet

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HiSilicon Technologies Co., Ltd.

Address: Huawei Industrial Base
Bantian, Longgang
Shenzhen 518129
People's Republic of China

Website: http://www.hisilicon.com

Email: support@hisilicon.com

# Hi3535 H.264 CODEC Processor

## Key Specifications

### Processor Core

- ARM Cortex A9 dual-core@ max. 1 GHz
  - 32 KB L1 I-cache, 32 KB L1 D-cache
  - 256 KB L2 cache

### Video Decoding Protocols

- H.264 baseline/main/high profile L5.0
- MPEG4 SP L0–3/ASP L0–5
- MJPEG/JPEG baseline

### Video Encoding Protocols

- H.264 baseline/main/high profile L4.2
- MJPEG/JPEG baseline

### Video Encoding/Decoding

- H.264&JPEG encoding and decoding of multiple streams:
  - 5x1080p@30 fps H.264 decoding+1x1080p@30 fps H.264 encoding +1080p@8 fps JPEG encoding
  - 9x720p@30 fps H.264 decoding+1x1080p@30 fps H.264 encoding+720p@16 fps JPEG encoding
  - 24xD1@30 fps H.264 decoding+1x1080@30 fps H.264 encoding+D1@32 fps JPEG encoding
  - 4x720p@30 fps JPEG decoding
- CBR or VBR, ranging from 16 kbit/s to 40 Mbit/s
- Encoding frame rate ranging from 1 fps to 60 fps
- ROI encoding
- Color-to-gray encoding

### Intelligent Video Engine

- Integrated IVE, supporting various intelligent analysis applications such as motion detection, boundary security, and video diagnosis

### Video and Graphic Processing

- Dynamic contrast enchantment and video pre- and post-processing such as deinterlacing, edge enhancement, 3D denoising, and dynamic contrast enhancement
- Anti-flicker for output videos and graphics
- 1/8x to 16x video scaling
- 1/2x to 2x graphic scaling
- Four cover regions
- OSD overlaying of eight regions
- Alpha blending of video layers and graphics layers

### Audio Encoding/Decoding

- Software encoding and decoding complying with multiple protocols

### Security Engine

- AES, DES, 3DES algorithms

### Video Interfaces

- VO interfaces
  - One HDMI 1.4 HD output interface
  - One VGA HD output interface
  - One BT.1120 HD output interface
  - Same source or difference sources for the HDMI and VGA interfaces
  - Same source for the BT.1120 and HDMI interfaces or BT.1120 and VGA interfaces
  - Maximum 1920 x 1200@60 fps for the VGA or HDMI interface
  - One CVBS SD output interface
  - Three full-screen GUI graphics layers in RGB1555 or RGB8888 format, used by two HD channels and one SD channel
  - One hardware cursor layer in RGB1555 or RGB8888 format, with the maximum resolution of 128 x 128

### Audio Interfaces

- One integrated audio CODEC, supporting 16-bit audio inputs and outputs
- Two unidirectional $I^2S$ interfaces
  - One input
  - One output
- External audio CODEC connected over the I2S interface, supporting 16- or 24-bit audio inputs and outputs

### Ethernet Ports

- Two gigabit Ethernet ports
  - RGMII, RMII, and MII modes
  - 10/100 Mbit/s full-duplex or half-duplex
  - 1000 Mbit/s full-duplex
  - TOE for reducing the CPU usage

### Peripheral Interfaces

- Two SATA 3.0 interfaces
  - PM
  - eSATA
- One PCIe 2.0/SATA 3.0 interface
  - RC and endpoint supported as the PCIe 2.0 interface
  - eSATA supported as the SATA 3.0 interface
- Four UART interfaces (including two 4-wire interfaces)
- One IR interface, one $I^2C$ interface, and multiple GPIO interfaces
- Two USB 2.0 host ports, supporting hub
- One USB 3.0 host port, supporting hub

### Memory Interfaces

- One 32-bit DDR3 SDRAM controller interface
  - Maximum frequency of 800 MHz (1.6 Gbit/s)
  - ODT
  - Maximum capacity of 2 GB
  - Automatic power consumption control
- SPI NOR flash interface
  - 1-, 2-, or 4-bit SPI NOR flash
  - Two CSs
  - Maximum capacity of 32 MB for each CS
- NAND flash interface
  - 8-bit NAND flash
  - SLC or MLC
  - 1-, 4-, 8-, or 24-bit ECC
  - Booting from the NAND flash
- Embedded 4 KB BOOTROM and 10 KB SRAM

### RTC with an Independent Power Supply

- Independent battery for supplying power to the RTC

### Configurable Boot Modes

- Booting from the BOOTROM
- Booting from the SPI NOR flash
- Booting from the NAND flash
- Booting from the DDR

### SDK

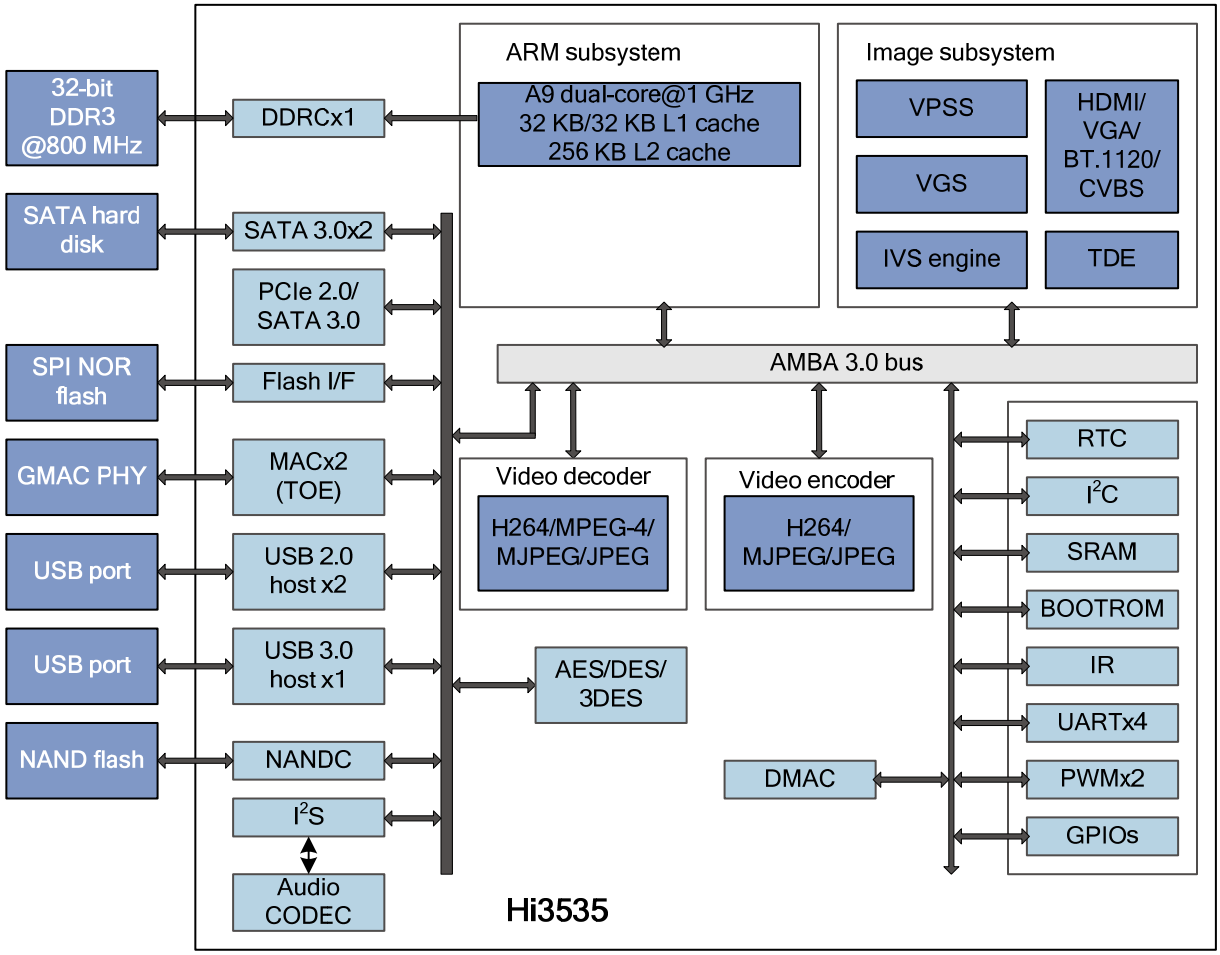
- Linux 3.4-based SDK
- High-performance H.264 PC decoding library

### Physical Specifications

- Power consumption
  - Typical power consumption of 3.5 W
  - Multi-level power-saving control
- Operating voltages
  - 1.1 V core voltage
  - 1.2 V CPU voltage (or decreased to 1.1 V)
  - 3.3 V I/O voltage
  - 1.5 V DDR3 SDRAM interface voltage
- Package
  - RoHS, EDHS-PBGA
  - Ball pitch of 0.8 mm (0.02 in.)
  - Body size of 23 mm x 23 mm (0.91 in. x 0.91 in.)

# Hi3535 H.264 CODEC Processor

## Functional Block Diagram




The Hi3535 is a professional SoC targeted for the multi-channel HD or D1 NVR. The Hi3535 provides a high-performance A9 processor, a video decoding engine (a maximum of 5x1080p decoding complying with various protocols), a high-performance video/graphics processing engine (various complicated graphics processing algorithms), and dual-channel HD outputs. These features enable the Hi3535 to provide high-quality images. In addition, the Hi3535 integrates various peripheral interfaces to meet differentiated customer requirements for functionality, features, and image quality, while reducing the eBOM cost.

## NVRs (Each with a Hi3535)

### 4x1080p NVR

- 5x1080p real-time decoding (4-channel preview and 1-channel playback)
- 1x1080p real-time encoding
- 1080p@8 fps JPEG snapshot
- HDMI+VGA 1080p@60 fps HD outputs+1xCVBS output

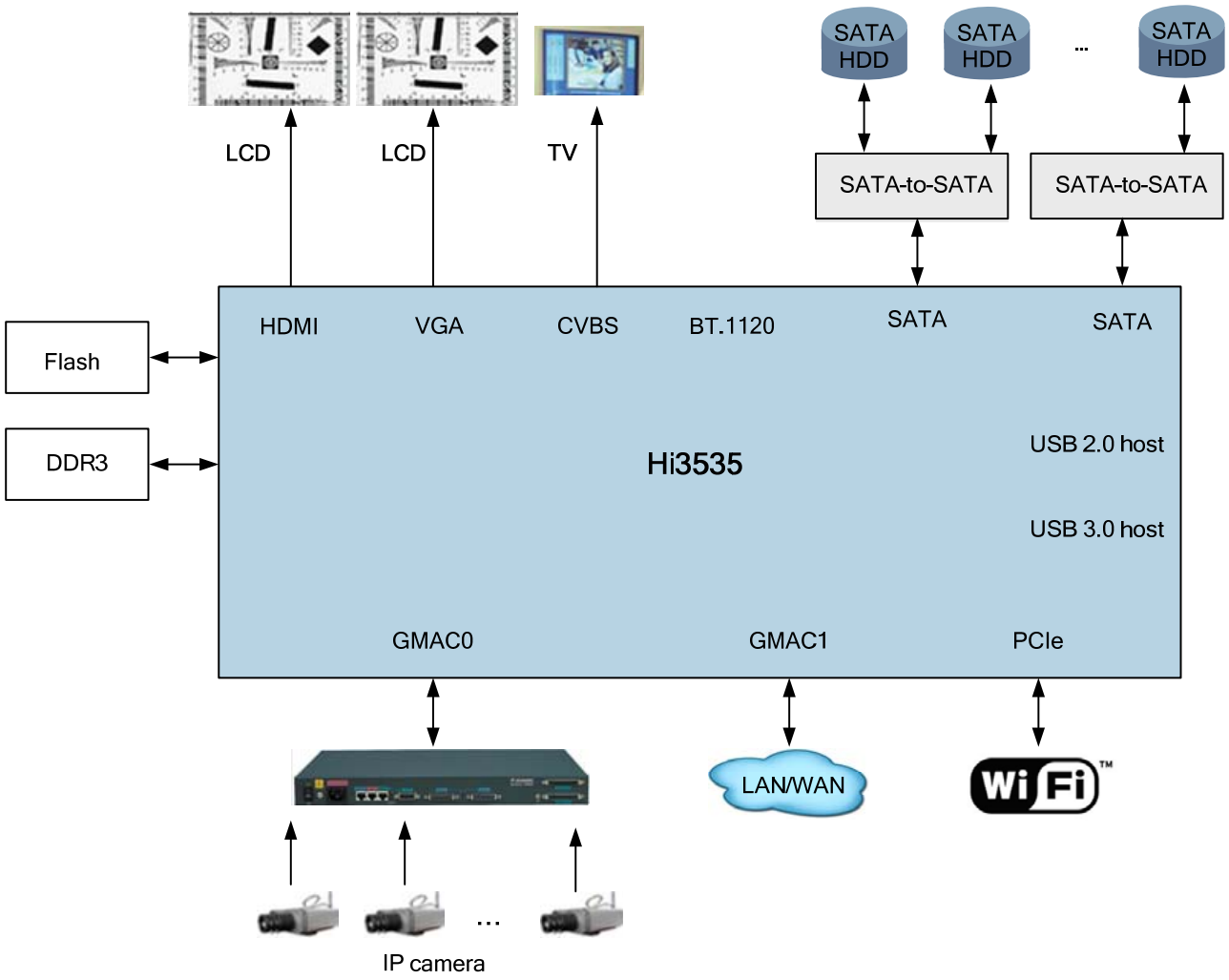
### 8x720p NVR

- 9x720p real-time decoding (8-channel preview and 1-channel playback)
- 1x1080p real-time encoding
- 720p@16 fps JPEG snapshot

- HDMI+VGA 1080p@60 fps HD outputs+1xCVBS output

**16xD1 NVR**

- 24xD1 real-time decoding (16-channel preview and +8-channel playback)
- 1x1080p real-time encoding
- D1@32 fps JPEG snapshot
- HDMI+VGA 1080p@60 fps HD outputs+1xCVBS output




# Acronyms and Abbreviations

| | |
|---|---|
| 3DES | triple data encryption standard |
| AES | advanced encryption standard |
| CBR | constant bit rate |
| CS | chip select |
| CVBS | composite video broadcast signal |
| DDR | double-data rate |
| DES | data encryption standard |
| ECC | error correcting code |
| eSATA | external serial advanced technology attachment |
| GPIO | general-purpose input/output |

| | |
|---|---|
| GUI | graphical user interface |
| HD | high-definition |
| HDMI | high-definition multimedia interface |
| $I^2C$ | inter-integrated circuit |
| $I^2S$ | inter-IC sound |
| IR | infrared |
| IVE | intelligent video engine |
| MII | media independent interface |
| MLC | multi-level cell |
| NVR | network video recorder |
| ODT | on-die termination |
| OSD | on-screen display |
| PBGA | plastic ball grid array |
| PCIe | peripheral component interconnect express |
| PM | port multiplexer |
| RC | root complex |
| RGMII | reduced gigabit media independent interface |
| RMII | reduced media independent interface |
| RoHS | restriction of the use of certain hazardous substances |
| ROI | region of interest |
| RTC | real-time clock |
| SATA | serial advanced technology attachment |
| SD | standard-definition |
| SDK | software development kit |
| SDRAM | synchronous dynamic random access memory |
| SLC | single-level cell |
| SoC | system-on-chip |
| SP | simple profile |
| SPI | serial peripheral interface |
| SRAM | static random access memory |
| TOE | TCP/IP offload engine |
| UART | universal asynchronous receiver transmitter |
| VBR | variable bit rate |
| VGA | video graphics array |
| VO | video output |